CLAIMS

Amend the claims as follows.

1. (Canceled)

2. (Currently amended) In a wireless receiver where~~in~~ a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, a method of automatic gain control (AGC) comprising:

(a) at a specified stage in an I/Q baseband strip containing multiple automatic gain control (AGC) stages, each of ~~said~~ the AGC stages having locally generated control signals associated therewith:

~~i.~~ detecting respective I and Q output signals received from respective I and Q variable gain amplifiers (VGAs) associated with ~~said~~ the specified AGC stage to produce a detected I and Q signal, the detecting comprising;

~~ii.~~ passing ~~said~~ the respective I and Q output signals through respective high pass filters (HPFs)~~;~~,

~~iii.~~ rectifying ~~said~~ each of the respective I and Q filtered output signals~~;~~,

~~iv~~ adding ~~said~~ the respective I and Q rectified filtered output signals in an operational amplifier~~;~~, and

~~v.~~ passing ~~said~~ the added I and Q rectified filtered output signal through a low pass filter (LPF) to produce the detected I and Q signal;

~~vi.~~ digitizing ~~said~~ the detected I and Q signals; and

~~vii.~~ adjusting with ~~said~~ the associated control signal ~~said~~ the respective I and Q VGAs for differences between ~~said~~ the detected I and Q ~~output~~ signals and a reference signal; ~~and~~

(b) repeating (a) through each AGC stage; and

where the digitizing comprises

receiving in an analog to digital converter (ADC) the detected I and Q signal,

comparing the detected I and Q signal to the reference signal, and

generating digital up/down and count/hold control signals.

3. (Canceled)

4. (Currently amended) The method of claim ~~3~~2 where~~in~~ ~~said~~ the ~~step of~~ comparing ~~further~~ comprises using a multi-level comparator and a logic circuit to generate ~~said~~ the digital up/down and count/hold control signals.

5. (Currently amended) The method of claim 4 where~~in~~ the ~~step of~~ adjusting ~~further~~ comprises:

~~(a)~~ receiving in an up/down counter ~~said~~ the digital up/down and count/hold control signals; and

~~(b)~~ setting the gains of the respective I and Q ~~variable gain amplifiers (~~VGAs~~)~~.

6. (Currently amended) The method of claim 5 where~~in~~ the ~~step of~~ setting ~~further~~ comprises:

~~(a)~~ if ~~said~~ the ~~I and Q filtered output~~ detected I and Q signal~~s~~ falls outside a predefined boundary, modifying the gains of ~~said~~ the respective I and Q VGAs until ~~a desired I/Q~~ the respective I and Q output signal~~s~~ ~~is~~ achieve~~d~~ desired magnitudes;

~~(b)~~ else, maintaining the gains of ~~said~~ the respective I and Q VGA~~s settings~~.

7. (Currently amended) The method of claim 6 where~~in~~ the ~~step of~~ modifying comprises adjusting ~~said~~ the respective I and Q VGAs at a fast rate if ~~said~~ the detected I/ and Q ~~output~~ signal is beyond a first predefined range or at a slow rate if ~~said~~ the detected I/ and Q ~~output~~ signal is beyond a second predefined range but not beyond the first predefined range.

8. (Currently amended) The method of claim 6 where~~in~~ the ~~step of~~ modifying comprises adjusting ~~said~~ the respective I and Q VGAs at a large magnitude if ~~said~~ the detected I/ and Q ~~output~~ signal is beyond a first predefined range or at a small magnitude if ~~said~~ the detected I/ and Q ~~output~~ signal is beyond a second predefined range but not beyond the first predefined range.

9. (Canceled)

10. (Currently amended) In a wireless receiver where a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, an automatic gain control (AGC) circuit comprising multiple AGC stages where each of the AGC stages includes:

(a) respective I and Q variable gain amplifiers (VGAs);

(b) a detector to detect respective I and Q output signals received from the respective I and Q VGAs and to produce a detected I and Q output signal;

(c) an analog to digital converter (ADC) to convert the detected I and Q output signals; ~~and~~

(d) a digital engine to digitally adjust the respective I and Q VGAs for differences between the detected I and Q output signals and a reference signal;

where the detector comprises:

i. respective I and Q high pass filters (HPFs) to remove direct current (DC) offsets from the respective I and Q output signals;

ii. ~~a~~ respective rectifiers communicating with the respective I and Q HPFs to change the respective filtered I and Q output signals from alternating current (AC) to direct current (DC);

iii. an operational amplifier (Op-amp) communicating with the rectifiers to add the rectified filtered I and Q output signals; and

iv. a low pass filter (LPF) communicating with the Op-amp to filter the added rectified filtered I and Q output signals to produce the detected I and Q output signal; and

where the ADC comprises a multi-level comparator and a logic circuit.

11. (Canceled)

12. (Currently amended) The automatic gain control circuit of claim ~~11~~10 where~~in~~ the number of levels in ~~said~~ the multi-level comparator is at least four.

13. (Currently amended) The automatic gain control circuit of claim 12 where~~in said~~ the digital engine comprises an up/down counter for setting gains associated with ~~said~~ the respective I and Q ~~variable gain amplifiers~~ (VGAs~~)~~.

14.-19. (Canceled)

20. (Currently amended) A wireless receiver including a plurality of serially connected automatic gain control stages, each stage comprising:

I and Q variable gain amplifiers (VGAs) to generate I and Q signals, respectively;

a detector to generate a detect signal ~~by detecting a difference between~~ from the I and Q signals;

an analog to digital converter (ADC) to convert the detect signal to a digital detect signal; ~~and~~

~~an~~ digital engine to generate a control signal responsive to the digital detect signal and a reference signal;

where the ADC is enabled to

compare the detect signal to the reference signal, and

generate digital up/down and count/hold control signals as the digital detect signal; and

where the I and Q VGAs operate responsive to the control signal.

21. (Currently amended) The wireless receiver of claim 20 comprising:

I and Q buffers amplifiers between the variable gain amplifiers and the detector to buffer the I and Q signals, respectively.

22. (Currently amended) The wireless receiver of claim 20 where the detector includes:

respective I and Q high pass filters to generate I and Q filtered signals by removing direct current offsets from the I and Q ~~output~~ signals.

23. (Currently amended) The wireless receiver of claim 22 where the detector includes:

~~a~~ respective rectifiers communicating with the respective I and Q high pass filters to change each of the I and Q filtered signals from alternating current to direct current, producing I and Q rectified filtered signals.

24. (Currently amended) The wireless receiver of claim 23 where the detector includes:

an operational amplifier to generate an added I and Q signals by adding the I and Q rectified filtered signals.

25. (Currently amended) The wireless receiver of claim 24 where the detector includes:

a low pass filter to filter the added I and Q signals to produce the detect signal.

~~25~~26. (Currently amended) A method comprising;

at each of a plurality of serially connected automatic gain control stages, each of the stages having a respective I variable gain amplifier with a respective I output signal and a respective Q variable gain amplifier with a respective Q output signal, generating a respective detect signal ~~by detecting a difference between~~ from the respective I and Q output signals ~~at respective outputs of I and Q variable gain amplifiers of a plurality of serially connected automatic gain control stages~~;

at each of the stages, converting the respective detect signal to a respective digital detect signal;

at each of the stages, generating a respective control signal to control the respective I and Q variable gain amplifiers responsive to the respective digital detect signal; ~~and~~

at each of the stages, adjusting the respective I and Q variable gain amplifiers responsive to the respective control signal; and

where the converting comprises comparing the respective detect signal to a respective reference signal via a multi-level comparator and a logic circuit.

~~26~~27. (Currently amended) The method of claim ~~25~~26 where the generating the respective detect signal ~~comprising~~ comprises:

generating respective I and Q filtered signals by removing direct current offsets from the respective I and Q output signals.

~~27~~28. (Currently amended) The method of claim ~~26~~27 where the generating the respective detect signal ~~comprising~~ comprises:

rectifying each of the respective I and Q filtered signals from alternating current to direct current to produce respective I and Q rectified filtered signals.

~~28~~29. (Currently amended) The method of claim ~~27~~28 where the generating the respective detect signal ~~comprising~~ comprises:

adding the ~~rectified~~ respective I and Q rectified filtered signals to produce a respective added I and Q rectified filtered signal.

~~29~~30. (Currently amended) The method of claim ~~28~~29 where the generating the respective detect signal ~~comprising~~ comprises:

low pass filtering the respective added I and Q rectified filtered signals ~~s~~ to produce the respective detect signal.

31. (New) The wireless receiver of claim 20

where the ADC comprises a multi-level comparator and a logic circuit;

where the multi-level comparator is enabled to compare the detect signal to the reference signal; and

where the logic circuit is coupled to the multi-level comparator and is enabled to generate the digital up/down and count/hold control signals.

32. (New) The method of claim 26 where the converting comprises generating digital up/down and count/hold control signals via the logic circuit.

33. (New) The method of claim 32 where the generating the respective control signal comprises:

(a) receiving in an up/down counter the digital up/down and count/hold control signals; and

(b) determining the respective control signal based, at least in part, on the value of the up/down counter.